REMARKS

Claims 1-20 are pending in the application. Claims 9-20 were withdrawn from consideration as being drawn to a non-elected invention.

In the Office Action, the abstract was objected to because the last sentence referred to "purported merits of the invention" (Office Action, page 2). The abstract has been amended to delete the last sentence. Approval of the abstract is respectfully requested.

Applicants' claimed invention is directed to a semiconductor package including at least one chip, and a plurality of conductive bumps deposited on respective bond pads of the chip. As recited in claim 1, an encapsulation body encapsulates the chip and the conductive bumps. A plurality of conductive traces are formed on the encapsulation body and electrically connected to exposed ends of the conductive bumps. Also, a solder mask layer is applied over the conductive traces and formed with openings for exposing predetermined portions of the conductive traces, the exposed portions being connected to a plurality of solder balls, respectively.

Applicants' claimed invention is exemplified by the following copy of FIG. 1.

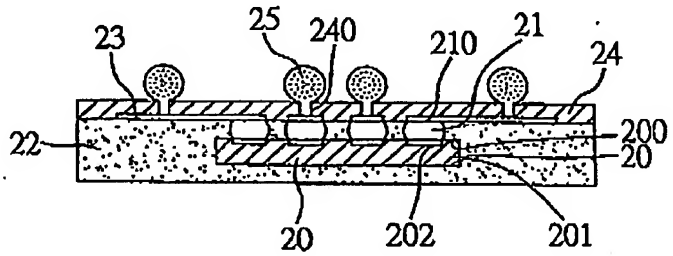

FIG. 1

As shown in FIG. 1, the semiconductor package includes at least one chip 20 and a plurality of bond pads 202 formed on the chip, where conductive bumps 21 are formed on respective bond pads 202. An encapsulation body 22 encapsulates the chip 20 and the conductive bumps 21. A plurality of conductive traces 23 are formed on the encapsulation body 22, and electrically connected to exposed ends 210 of the conductive bumps 21.

Claims 1, 2, and 5-8 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,701,614 to Ding et al. (hereinafter "Ding"). Claims 3 and 4 were rejected under 35 USC 103(a) as being unpatentable over Ding in view of U.S. Patent 6,734,534 to Vu et al. (hereinafter "Vu"). These rejections are respectfully traversed.

Ding does not teach or suggest a semiconductor package including: an encapsulation body for encapsulating a chip and a plurality of conductive bumps, and a plurality of first conductive traces formed on the surface of the encapsulation body.

Ding discloses a method for making a build-up package having a semiconductor die 30. As shown in FIG. 4b, a copper foil 50 bonded with conductive columns 51 and a dielectric film 60 are "thermally compressed onto the surface 41 of the encapsulating material 40" (column 4, lines 7-8), so that the conductive columns 51 penetrate the dielectric film 60 until bonding on bond pads 34 of the die 30 (see column 4, lines 5-24).

In the Office Action, reference numerals 40 and 61 were cited as corresponding to the Applicants' claimed "encapsulation body". However, only reference numeral 40 corresponds to an encapsulation body – as taught in Ding: "the surface 41 of the encapsulating material 40 is planar for building up dielectric layers and conductive traces" (column 4, lines 2-4). As shown in FIG. 4h, e.g., reference numerals 61 and 81 correspond to first and second dielectric layers, respectively.

In other words, the first dielectric layer 61 in Ding is **not** part of an encapsulation body. As explained in column 4, lines 32-40 of Ding, "the first dielectric film 60 is cured to become a C-staged polymer for forming a first dielectric layer 61", where the first dielectric layer 61 has a different coefficient of thermal expansion (CTE) than the encapsulating material 40. Therefore, the first dielectric layer 61 in Ding cannot be considered part of an "encapsulation body".

Moreover, the difference in CTE between the chip, dielectric layer, and encapsulating material in Ding would likely cause delamination problems (see discussion in Background section of the application at page 3, last paragraph). Also, by thermally compressing the copper foil 50 and the dielectric film 60 onto the surface of the encapsulating material 40, one would likely expect circuit breaks due to misalignment of the conductive column with the chip bond pads since locations of the chip bond pads are not easily identified with the first dielectric layer 61 formed on the surface of the encapsulating material 40.

Ding also does not teach or suggest "a plurality of first conductive traces formed on the surface of the encapsulation body," as recited in claim 1.

In the Office Action, conductive traces 72 were cited as corresponding to the Applicants' claimed "first conductive traces". However, as shown in FIGS. 4f to 4h, the conductive traces 72 are electrically connected to respective conductive columns 71 disposed **on a second dielectric layer 81** (see column 5, lines 3-14). Therefore, the conductive traces 72 are not formed on the surface of the encapsulation body/material 40, as recited in claim 1.

For at least the reasons discussed above, Ding does not anticipate or otherwise render obvious the Applicants' claimed invention.

Accordingly, claim 1 is patentably distinguishable over the Ding reference. For at least the same reasons, claims 2-8 also are patentable over Ding.

Regarding claims 3 and 4, the Vu reference fails to remedy the above-mentioned deficiencies of Ding. Vu was cited for teaching an inactive surface 118 of a chip 114 being exposed outside of an encapsulation body 122. However, Vu does not teach or suggest an encapsulation body for encapsulating a chip and a plurality of conductive bumps. Therefore, even if Vu were combined with Ding, the proposed combination still would not teach or suggest the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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